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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,703	10/23/2003	Shih-Chang Chang	LEE0023-US	9727

7590 07/20/2006

Michael D. Bednarek
Shaw Pittman LLP
1650 Tysons Boulevard
McLean, VA 22102

EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,703	CHANG ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *1-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. This application contains claims 1-16 are drawn to an invention nonelected withtraverse in the reply filed on 7/28/2005. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kouyuu et al. [JP 11097703] newly cited.

With respect to claim 14, Kouyuu et al. (fig. 9D-9E) discloses a semiconductor device with a lightly doped region, comprising:

a substrate (801, 802, 803, 804) with a first area and a second area;

a first type thin film transistor formed in said first area; and

a second type thin film transistor formed in said second area;

wherein said first type thin film transistor comprises:

first source/drain regions (815, 816) formed in said substrate (803) and separated by a first channel (819);

a first gate dielectric layer (805) formed on said substrate (803) covering said first channel (819);

a first gate electrode (806) formed on said first gate dielectric layer corresponding to said first channel;

a spacer (814) formed on a sidewall of said first gate electrode (806); and

a lightly doped region (817 and 818) formed in a portion of said source/drain region (815, 816) corresponding to said spacer (814); and

wherein said second type thin film transistor comprises:

second source/drain regions (810, 811) formed in said substrate (804) and separated by a second channel (813);

a second gate dielectric layer (805) formed on said substrate (804) covering said second channel (813) and a sides of said second source/drain regions (810, 811); and

a second gate electrode (807) formed on said second gate dielectric layer corresponding to said second channel (813);

wherein said second type thin film transistor, without any spacer and any lightly doped region, is different from said first type thin film transistor.

With respect to claim 15, Kouyuu et al. (fig. 9D-9E) discloses that said first and second type thin film transistors comprises an n-type and a p-type thin film transistors.

With respect to claim 16, Kouyuu et al. (text 0032) discloses that said first and second gate dielectric layers (1105) are selected from the group consisting of a nitride layer, an oxide layer, and a combination thereof.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 14-16, insofar clear, are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. [U.S. 6,635,505] previously applied.

With respect to claim 14, Tanaka et al. (figs. 11A-12C, cols. 13-15) discloses a semiconductor device with a lightly doped region, comprising:

a substrate (1101, 1102, 1103, 1104) with a first area and a second area;

a first type thin film transistor formed in said first area; and

a second type thin film transistor formed in said second area;

wherein said first type thin film transistor comprises:

first source/drain regions (1119) formed in said substrate (1103) and separated by a first channel (1110);

a first gate dielectric layer (1105) formed on said substrate (1103) covering said first channel;

a first gate electrode (1106) formed on said first gate dielectric layer corresponding to said first channel;

a spacer (1112) formed on a sidewall of said first gate electrode (1106); and

a lightly doped region (1108 and 1114) formed in a portion of said source/drain region (1119) corresponding to said spacer (1112); and

wherein said second type thin film transistor comprises:

second source/drain regions (1123) formed in said substrate (1104) and separated by a second channel (1111);

a second gate dielectric layer (1105) formed on said substrate (1104) covering said second channel (1111) and a portion of said second source/drain regions (1123); and

a second gate electrode (1107) formed on said second gate dielectric layer corresponding to said second channel (1111);

wherein said second type thin film transistor, without any spacer and any lightly doped region, is different from said first type thin film transistor.

With respect to claim 15, Tanaka et al. (fig. 12C and col. 15, lines 32-37) discloses that said first and second type thin film transistors comprises an n-type and a p-type thin film transistors.

With respect to claim 16, Tanaka et al. (fig. 11a and col. 13, lines 50-54) discloses that said first and second gate dielectric layers (1105) are selected from the group consisting of a nitride layer, an oxide layer, and a combination thereof.

Response to Arguments

7. Applicant's arguments with respect to claims 14-16 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed May 08, 2006 have been fully considered but they are not persuasive.

Applicant argues that the gate insulating film (1122) of Tanaka does not cover the impurity region (1123).

Applicant's argument is not persuasive because Tanaka clearly discloses the gate insulating film (1122) covers a top portion of the impurity region (1123) (see fig. 12C).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER